CLAIMS

What is claimed is:

1. A processor comprising:

a voltage supply input port to receive a voltage at a first voltage level; and

a cache to flush or maintain, depending on a power status signal, its contents upon entering a low power state in which the voltage is to be received at a second voltage level, the second voltage level being lower than the first voltage level.

2. The processor of claim 1, wherein the voltage supply input port is coupled to the cache to power the cache, and the second voltage level is less than twice an average threshold voltage of a majority of transistors of the processor.

3. The processor of claim 1, further comprising:

a power status signal port to receive the power status signal from an external source; and

a core to receive the power status signal and to flush or maintain the contents of the cache depending on the power status signal.

4. The processor of claim 1, further comprising a core to generate the power status signal and to flush or maintain the contents of the cache depending on the power status signal.

5. The processor of claim 1, further comprising:

a core to execute instructions; and

a phase locked loop to provide a clock signal to the core, the clock signal to be off during the low power state.

6. The processor of claim 1, wherein the cache is an L1 cache, an L2 cache, or both.

7. The processor of claim 1, wherein the cache is to flush its contents upon entering the low power state if the power status signal indicates that a system in which the processor resides is to be suspended.

8. The processor of claim 1, wherein the cache is to flush its contents upon entering the low power state if the power status signal indicates that power reduction associated with maintaining the contents of the cache upon entering the low power state is a lower priority than avoiding an increase in a soft error rate in the cache associated with reducing the voltage to the second voltage level.

9. The processor of claim 8, wherein the power status signal indicates that power reduction associated with maintaining the contents of the cache upon entering the low power state is a lower priority than avoiding an increase in a soft error rate in the cache associated with reducing the voltage to the second

voltage level if the power status signal indicates that the voltage is being provided by an electrical power outlet.

10. The processor of claim 1, wherein the cache is to maintain its contents upon entering the low power state if the power status signal indicates that power reduction associated with maintaining the contents of the cache upon entering the low power state is a higher priority than avoiding an increase in a soft error rate in the cache associated with reducing the voltage to the second voltage level.

11. The processor of claim 10, wherein the power status signal indicates that power reduction associated with maintaining the contents of the cache upon entering the low power state is a higher priority than avoiding an increase in a soft error rate in the cache associated with reducing the voltage to the second voltage level if the power status signal indicates that the voltage is being provided by a battery.

12. A computer system comprising:

a voltage regulator to supply a voltage at a first voltage level and to supply the voltage at a lower second voltage level while in a low power state;

a cache, to be powered by the voltage from the voltage regulator; and

a power manager to send a first or second signal if power reduction associated with maintaining contents of the cache upon entering the

low power state is a lower or higher priority, respectively, than avoiding an increase in a soft error rate in the cache associated with the low power state.

13. The computer system of claim 12, wherein the cache is to flush or maintain its contents if the processor receives the first or second signal, respectively, upon entering the low power state.

14. The computer system of claim 13, further comprising a clock to provide a clock signal to a core of a processor containing the cache, the clock signal to the core to be off during the low power state.

15. The computer system of claim 13, wherein the second voltage level is less than twice an average threshold voltage of a majority of transistors of the cache.

16. The computer system of claim 12, wherein the second voltage level is less than twice an average threshold voltage of a majority of transistors of the cache.

17. A computer system comprising:

a voltage regulator to supply a voltage;

a clock to provide a clock signal; and

a processor to receive the clock signal and the voltage, the processor including a cache, the processor to flush or maintain, depending on a power status signal, contents of the cache upon entering a low power state in which the clock is off and the voltage is reduced.

18. The computer system of claim 17, wherein the voltage regulator is to supply the voltage at a voltage level that is less than twice an average threshold voltage of a majority of transistors of the cache during the low power state.

19. The computer system of claim 17, wherein the voltage regulator is to supply the voltage to the processor at a reduced voltage level during the low power state, and the cache is to flush its contents upon entering the low power state if the power status signal indicates that the computer system is to be suspended.

20. The computer system of claim 19, wherein the cache is to maintain its contents upon entering the low power state if the power status signal indicates that the voltage is being provided by a battery.

21. The computer system of claim 20, wherein the cache is to flush its contents upon entering the low power state if the power status signal indicates that the voltage is being provided by an electrical power outlet.

22. A method comprising:

triggering a processor of a computer system to enter a low power state in which a voltage supplied to a cache of the processor is reduced and a clock supplied to the processor is off; and

flushing or maintaining contents of the cache upon entering the low power state depending on a power status signal.

23. The method of claim 22, further comprising flushing the contents of the cache upon entering the low power state if the computer system is to be suspended

24. A machine-readable medium including machine-readable instructions that, if executed by a machine, cause the machine to perform the method of claim 22.

25. A machine-readable medium including machine-readable instructions that, if executed by a machine, cause the machine to perform the method of claim 23.